



Electromigration Modeling at Circuit Layout Level (SpringerBriefs in Applied Sciences and Technology)

By Cher Ming Tan, Feifei He

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Integrated circuit (IC) reliability is of increasing concern in present-day IC technology where the interconnect failures significantly increases the failure rate for ICs with decreasing interconnect dimension and increasing number of interconnect levels. Electromigration (EM) of interconnects has now become the dominant failure mechanism that determines the circuit reliability. This brief addresses the readers to the necessity of 3D real circuit modelling in order to evaluate the EM of interconnect system in ICs, and how they can create such models for their own applications. A 3-dimensional (3D) electro-thermo-structural model as opposed to the conventional current density based 2-dimensional (2D) models is presented at circuit-layout level.

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